

REMARKS

Claims 1-12 are pending in this application. Claims 1, 11, and 12 are independent. In light of the remarks contained herein, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1-3 under 35 U.S.C. §102(b) as being anticipated by *Parulski et al.* (USP 5,668,597); rejected claims 4-7 and 9-12 under 35 U.S.C. §103(a) as being unpatentable over *Harada et al.* (USP 6,108,036) in view of *Parulski et al.*; and rejected claim 8 under 35 U.S.C. §103(a) as being unpatentable over *Harada et al.* in view of *Parulski et al.* and further in view of *Dischert* (USP 6,040,869). Applicant respectfully traverses these rejections.

**Claim Rejections - 35 U.S.C. §102(b) - *Parulski et al.***

With regard to the Examiner's rejection of claim 1, the Examiner asserts *Parulski et al.* teaches a solid imaging device that includes pixel information of two adjoining lines with color information of three primary colors citing to Fig. 3. The Examiner further asserts *Parulski et al.* teaches that a line-skipping pattern may be implemented when images of lower resolution are suitable, citing to col. 6, lines 56-57, col. 7, lines 3-14, and Figs. 10-11. Applicant respectfully disagrees with the Examiner's characterization of this reference.

The disclosure of *Parulski et al.* is directed to an electronic camera with rapid automatic focus of an image upon a progressive scan image sensor. The automatic focus of the lens employs a progressive scan image sensor 20 with a fast dump structure 62 (Abstract). Specifically, *Parulski et al.* teaches at col. 5, lines 24-38 as follows:

The sensor 20 uses a progressive scan readout method, which allows the entire image to be read out in a single scan. In this operating mode, all of the pixels on the sensor are transferred to the horizontal register 60, which delivers the image signals to the analog gain and CDS circuit 32 (see FIG. 1). More specifically, referring to FIG. 2A, the accumulated or integrated charge for the photodiodes comprising the photosites 58 is transported from the photosites to light protected vertical (parallel) registers 59 by applying a large positive voltage to the phase-one vertical clock (V1). This reads out every row, or line, into the vertical registers 59. The charge is then transported from the vertical registers 59 to the horizontal register 60 by two-phase clocking of the vertical clocks (V1, V2). Between the vertical and horizontal registers is the fast dump structure 62,...

Additionally, *Parulski et al.* teaches at col. 7, lines 3-14 as follows:

...The line-skipping pattern for the central focusing area 66 is shown in FIG. 10. The first two lines (1 and 2) are read out as in the imaging mode. These provide a green-red and a blue-green line. The next two lines (3 and 4) are eliminated by turning on the fast dump structure 62 during the time that these lines are transferred past the fast dump structure 62. Next, lines 5 and 6 are read out normally, and then lines 7 and 8 are eliminated through the fast dump structure 62. This process proceeds through the central area 66 and generates an output image signal having the Bayer-type color filter repeating pattern, so that the signals can be processed using algorithms designed for the Bayer pattern.

In contrast, the present invention set forth in claim 1 recites, *inter alia*, a solid imaging device comprising transferring gates to which gate pulses for transferring only the pixel information of pairs of two adjoining lines with intervals of a plurality of lines to vertical transferring routes are applied when image signals with low definition are produced. As noted above, *Parulski et al.* teaches transferring all pixel information to fast dump gate 62, where certain line information is decimated.

Additionally, *Parulski et al.* teaches as follows: "This reads out every row, or line, into the vertical registers 59." (Col. 5, lines 33-34) (emphasis added). That is, all of the pixels on the sensor are transferred to the vertical registers 59. This operation requires a considerably longer time, and the "fast dump structure" does not make any contribution to reduction in the operation time.

Additionally, *Parulski et al.* teaches as follows:

By setting a suitable positive potential on a fast dump gate line FDG, charge from the row (line) of pixel values currently adjacent to the fast dump structure 62 is transferred from the CCD channel directly into the sensor substrate 64 rather than to the horizontal register 60. (Col. 5, lines 40-44) (emphasis added).

and

When properly controlled by the sensor timing circuit 28, the fast dump structure 62 allows lines of charge to be eliminated. (Col. 5, lines 46-48) (emphasis added).

In *Parulski et al.*, there is a problem of the residual charge in the lines where the charge has been subject to be eliminated.

The residual charge causes pixels to be mixed (impure) between the lines. In order to completely eliminate the residual charge, a high voltage supply device is necessary to make the positive potential high, and/or it is necessary to spend a long time to eliminate the charge.

In contrast, the solid imaging device according to the present invention is free from the above-mentioned problems, since it comprises transferring gates to which gate pulses for transferring only the pixel information of pairs of two adjoining lines with intervals of a plurality of lines to vertical transferring routes are applied when image signals with low definition are produced. As such, *Parulski et al.* fails to teach transferring gates to which gate pulses for transferring **only** pixel information of pairs of two adjoining lines with intervals of a plurality of lines to vertical transferring routes are applied as set forth in claim 1.

As *Parulski et al.* fails to teach or suggest all elements of claim 1, it is respectfully submitted that *Parulski et al.* fails to anticipate the present invention of claim 1. As such, it is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 2-10 are allowable for the reasons set forth above with regard to claim 1 at least based upon their dependency on claim 1.

Claim Rejections - 35 U.S.C. §103(a) -  
*Harada et al./Parulski et al.*

In support of the Examiner's rejection of claim 11, the Examiner admits that *Harada et al.* fails to teach or suggest applying gate pulses for transferring only pixel information of pairs of two adjoining lines with intervals of a plurality of lines to said vertical transferring routes to said transferring gates when image signals with low definition are produced. The Examiner relies on the teachings of *Parulski et al.* to cure the deficiencies of the teachings of *Harada et al.* However, as noted above, *Parulski et al.* fails to teach or suggest this claim element. As neither of the references cited by the Examiner teach or suggest this claim element, either alone or in combination (assuming these references are combinable, which Applicant does not admit), the Examiner has failed to establish *prima facie* obviousness. It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claim 12 includes elements similar to those discussed above with regard to claim 11 and, thus, claim 12 is not obvious over *Harada et al.* in view of *Parulski et al.* for the reasons set forth above with regard to claim 11.

Conclusion

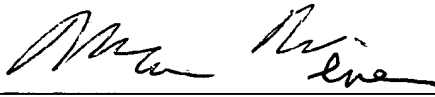
Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinnet (Reg. No. 52,327) at the


telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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